ABSTRACT

A system for use with a multi-phase clock generator is disclosed. It should also be understood that the multiphase clock generator can be a phase lock loop (PLL), delay lock loop (DLL), or any other circuit capable of providing a multiphase clock. The system comprises at least two phase detectors coupled to the multi-phase clock generator for receiving component clock signals of the multi-phase clock generator, wherein at least some of the component clock signals are offset from each other in phase. Each of the phase detectors detects phase differences between pairs of component clock signals. The system includes a summer coupled to the at least two phase detectors for measuring the phase differences between the at least two phase detectors. The system includes at least one variable delay element for receiving the measured phase difference and for providing a delay which is proportional to an output value of the summer. The delay is used to reduce the phase differences.